Electronic Version
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Claims

[c1] 1. A method for testing integrated circuit devices after manufacture, said method comprising:

testing a group of devices to produce a failing group of devices that failed said testing, wherein said devices in said failing group are identified by type of failure; and

retesting only devices in said failing group that have a type of defect approved for retesting.

[c2] 2. The method in claim 1, further comprising retesting devices having types of defects associated with testing.

[c3] 3. The method in claim 1, wherein said testing process comprises probe type testing.

[c4] 4. The method in claim 1, wherein said devices comprise integrated circuit chips.

[c5] 5. The method in claim 1, wherein said retesting process is optimized by only retesting devices in said failing group that have said type of defect approved for retesting.

[c6] 6. The method in claim 1, wherein a listing of types of

defects approved for retesting comprises an optimized retest table.

[c7] 7. The method in claim 1, wherein said type of defect approved for retesting is based upon previously acquired statistics of previous testing the same type of device.

[c8] 8. A method for testing integrated circuit devices after manufacture, said method comprising:

testing an initial group of devices to produce an initial failing group of devices that failed said testing of said initial group, wherein said devices in said initial failing group are identified by type of failure;

retesting said devices in said initial failing group to identify a retested passing group of devices that passed said retesting;

analyzing said devices in said retested passing group to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure;

evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce types of defects approved for retesting;

testing additional groups of devices to produce additional failing groups of devices that failed said testing of said additional groups; and

retesting only devices in said additional failing groups that have one of said types of defects approved for retesting.

[c9] 9. The method in claim 8, further comprising adding types of defects associated with testing errors to said types of defects approved for retesting.

[c10] 10. The method in claim 8, wherein said testing processes comprise probe type testing.

[c11] 11. The method in claim 8, wherein said devices comprise integrated circuit chips.

[c12] 12. The method in claim 8, wherein said evaluating process optimizes said retesting of said additional groups.

[c13] 13. The method in claim 8, wherein a listing of said types of defects approved for retesting comprises an optimized retest table.

[c14] 14. The method in claim 8, wherein said initial group of devices and said additional groups of devices comprise the same type of device.

[c15] 15. A method for testing integrated circuit devices after manufacture, said method comprising:

testing an initial group of devices to produce an initial failing group of devices that failed said testing of

said initial group, wherein said devices in said initial failing group are identified by type of failure;

retesting said devices in said initial failing group to identify a retested passing group of devices that passed said retesting;

analyzing said devices in said retested passing group to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure;

evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce types of defects approved for retesting;

testing additional groups of devices to produce additional failing groups of devices that failed said testing of said additional groups;

identifying types of devices having a predetermined reduced demand; and

retesting only devices in said additional failing groups that have one of said types of defects approved for retesting, without retesting types of devices for which there is said predetermined reduced demand.

[c16] 16. The method in claim 15, further comprising adding types of defects associated with testing errors to said

types of defects approved for retesting.

[c17] 17. The method in claim 15, wherein said testing processes comprise probe type testing.

[c18] 18. The method in claim 15, wherein said devices comprise integrated circuit chips.

[c19] 19. The method in claim 15, wherein said evaluating process optimizes said retesting of said additional groups.

[c20] 20. The method in claim 15, wherein a listing of said types of defects approved for retesting comprises an optimized retest table.

[c21] 21. The method in claim 15, wherein said initial group of devices and said additional groups of devices comprise the same type of device.

[c22] 22. A system for testing integrated circuit devices after manufacture, said system comprising:

a tester adapted to test devices;

a database comprising types of defects approved for retesting, wherein said types of defects approved for retesting are based upon previously acquired statistics of which types of failures have retest passing rates, after initially failing testing, above a predeter-

mined threshold; and

a processor in communication with said tester and said database, wherein said processor is adapted to direct said tester to test groups of devices to produce failing groups of devices that failed the testing, wherein said processor is further adapted to direct said tester to retest only devices in said additional failing groups that have one of said types of defects approved for retesting.

[c23] 23. The system in claim 22, wherein said database includes types of defects associated with testing errors within said types of defects approved for retesting.

[c24] 24. The system in claim 22, wherein said tester comprise a probe-type tester.

[c25] 25. The system in claim 22, wherein said devices comprise integrated circuit chips.

[c26] 26. The system in claim 22, wherein said processor optimizes said retesting of said devices when controlling said tester.

[c27] 27. The system in claim 22, wherein said database comprises an optimized retest table.

[c28] 28. The system in claim 22, wherein said statistics of

said types of defects relate to the same type of device being tested.

[c29] 29. A system for testing integrated circuit devices after manufacture, said system comprising:

means for testing an initial group of devices to produce an initial failing group of devices, wherein said devices in said initial failing group are identified by type of failure;

means for retesting said devices in said initial failing group to identify a retested passing group of devices;

means for analyzing said devices in said retested passing group to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure; and

means for evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce types of defects approved for retesting;

means for testing additional groups of devices to produce additional failing groups of devices; and

means for retesting only devices in said additional failing groups that have one of said types of defects approved for retesting.

[c30] 30. A program storage device readable by machine, tangibly embodying a program of instructions executable by

the machine to perform a method of testing integrated circuit devices after manufacture, said method comprising:

testing a group of devices to produce a failing group of devices that failed said testing, wherein said devices in said failing group are identified by type of failure; and

retesting only devices in said failing group that have a type of defect approved for retesting.

[c31] 31. The program storage device in claim 30, wherein said method further comprises retesting devices having types of defects associated with testing.

[c32] 32. The program storage device in claim 30, wherein said testing process comprises probe type testing.

[c33] 33. The program storage device in claim 30, wherein said devices comprise integrated circuit chips.

[c34] 34. The program storage device in claim 30, wherein said retesting process is optimized by only retesting devices in said failing group that have said type of defect approved for retesting.

[c35] 35. The program storage device in claim 30, wherein a listing of types of defects approved for retesting comprises an optimized retest table.

[c36] 36. The program storage device in claim 30, wherein said type of defect approved for retesting is based upon previously acquired statistics of previous testing the same type of device.